[JP,2001-150398,A]

CLAIMS

[Claim(s)]
[Claim 1]It is a joining method of a silicon wafer which piles up the 1st silicon substrate in which a circuit element was formed, and the 2nd silicon substrate used as a plinth, and is joined, A diffusion prevention layer which prevents diffusion of Au to said 1st silicon substrate is formed, Form an Au layer on it and a diffusion prevention layer which prevents diffusion of Au to said 2nd silicon substrate is formed, A joining method of a silicon wafer forming an Au layer on it, piling up the Au layers of said 1st and 2nd silicon substrates, applying predetermined load and temperature, and joining the Au layers of both silicon substrates.
[Claim 2]A joining method of the silicon wafer according to claim 1 forming said diffusion prevention layer with a metal thin film containing any at least one of Ti, nickel, Cr, W, and the aluminum.
[Claim 3]A joining method of the silicon wafer according to claim 1 forming said diffusion prevention layer by silicon oxide.
[Claim 4]A joining method of the silicon wafer according to claim 1 forming said diffusion prevention layer with a silicon nitride film.
[Claim 5]A joining method of the silicon wafer according to claim 1 forming said diffusion prevention layer with a glass thin film by sputtering.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]In the manufacturing process of micromachines, such as a piezoresistance type semiconductor pressure sensor, an acceleration sensor, and an actuator, this invention relates to the method of joining silicon substrates in detail about the joining method of a silicon wafer.
[0002]
[Description of the Prior Art]Drawing 4 shows the structure of the piezoresistance type semiconductor pressure sensor as an example of the micromachine with which this invention is applied. This sensor has the work which takes out distortion of the sensor chip produced with minute pressure as an electrical signal. The sensor body which consists of the sensor chip 21 and the plinth glass 22 is being fixed to the plastic package 23 with the silicone or the epoxy adhesive 24 of low stress. The breakthrough 25 which introduces the pressure of a fluid into the sensor chip 21 is formed in the plastic package 23 and the plinth glass 22. The closing-in part (diaphragm part) 26 of the sensor chip 21 is equipped with the piezoresistive element (not shown) which changes into an electrical signal distortion produced with the pressure of a fluid. The plastic package 23 is PURIMORUDO the lead 27 and electrical connection of a piezoresistive element and the lead 27 is carried out with gold or the wire 28 made from aluminum.
[0003]Drawing 5 shows an example of the manufacturing process of the sensor body which consists of the above sensor chips 21 and the plinth glass 22. The sensor board (wafer) 31 in which two or more sensor chips containing the diaphragm part 33 and the piezoresistive element 34 were formed, and the glass substrate 32 made from Pyrex glass equivalent to two or more plinth glass with which the breakthrough 35 was formed are joined by anode joining. Then, it can carve into each sensor body by dicing. Thus, by manufacturing the sensor body which consists of the sensor chip 21 shown in drawing 4, and the plinth glass 22, the influence of the stress from the plastic package 23 is suppressed, and highly precise-ization of the sensor chip 21 is attained.
[0004]Anode joining of the sensor board 31 and the glass substrate 32 is performed by impressing about [400-1000V] direct current voltage between the glass substrate 32 and the sensor board 31, and impressing hundreds of g load in a vacuum or a nitrogen atmosphere of about 300-500 **. The lower heater electrode 36 is formed in the glass substrate 32 side, and it maintains to 0V potential. On the other hand, the anode pin 37 is formed in the sensor board 31 side, and about [400-1000V] direct current voltage is impressed.
[0005]
[Problem(s) to be Solved by the Invention]In the method of joining the sensor board 31 and the glass substrate 32 by the above anode joining, there was a problem resulting from the slight difference with the coefficient of thermal expansion of the glass substrate 32 and the coefficient of thermal expansion of the sensor board (silicon wafer) 31 used as plinth glass. That is, since the stress resulting from the difference in the above-mentioned coefficient of thermal expansion is inherent in the sensor body which consists of the sensor chip 21 which carved the sensor board 31 and the glass substrate 32 which were joined, and was made by dicing, and the plinth glass 22, a sensor body has offset voltage. Change of the temperature characteristics of an output span cannot be disregarded, either.

[0006]Then, it is possible to replace with plinth glass and to form a plinth with the silicon wafer of the same construction material as the sensor board 31. In this case, methods of joining the silicon substrate (henceforth a plinth board) used as the sensor board 31 and a plinth include the method by Au-Si eutectic bonding.
[0007]Drawing 6 shows junction to the sensor board 31 and the plinth board 41 by Au-Si eutectic bonding. First, Au layer 42 is formed in the plane of composition of the sensor board 31 by sputtering or vacuum evaporation at a thickness of several micrometers. Then, Au-Si eutectic bonding is formed by impressing the load of severalkilogram[/cm] ^{2} to tens kg/cm^2 for Au layer 42 of the sensor board 31, and the plane of composition of the plinth board 41 in piles in the atmosphere of a temperature (about 400 **) higher than the Au-Si eutectic temperature of 363 **.
[0008]Thus, if a plinth is formed with the silicon wafer of the same construction material as the sensor board 31, the problem resulting from the difference in the coefficient of thermal expansion in the case of forming a plinth with glass like before will be solved.
[0009]However, in the case of Au-Si eutectic bonding, as an arrow shows in drawing 6, Au atom in Au layer 42 is spread inside [of the sensor board 31 and the plinth board 41] silicon bulk, and, as a result, there is another problem that a void occurs in a plane of composition. When a void occurs in a plane of composition, there is a possibility that bonding strength may become weak and exfoliation by a joining interface may arise.
[0010]Like [in the case of this invention solving the above problems and forming a plinth with the silicon wafer of the same construction material as a sensor board in a pressure sensor], When joining silicon substrates, generating of the void in a plane of composition is suppressed, and it aims at providing the joining method of a silicon wafer without fear, such as exfoliation by a joining interface.
[0011]
[Means for Solving the Problem]The 1st silicon substrate in which a circuit element was formed as for a joining method of a silicon wafer by this invention, When piling up the 2nd silicon substrate used as a plinth and joining, a diffusion prevention layer which prevents diffusion of Au to the 1st silicon substrate is formed, An Au layer is formed on it, a diffusion prevention layer which prevents diffusion of Au to the 2nd silicon substrate is formed, an Au layer is formed on it, the Au layers of the 1st and 2nd silicon substrates are piled up, predetermined load and temperature are applied, and the Au layers of both silicon substrates are joined.
[0012]According to the above joining methods, diffusion inside the 1st or 2nd silicon substrate of Au atom in an Au layer is controlled by diffusion prevention layer formed in each silicon substrate. As a result, generating of a void in a plane of composition is suppressed, and firm junction is realized.
[0013]As for the above-mentioned diffusion prevention layer, it is preferred to form with a metal thin film containing any at least one of Ti, nickel, Cr, W, and the aluminum. Or it is also preferred to form a diffusion prevention layer with silicon oxide or a silicon nitride film. A diffusion prevention layer may be formed with a glass thin film by sputtering.
[0014]
[Embodiment of the Invention]Hereafter, the embodiment of this invention is described, referring to drawings.
[0015]Drawing 3 shows the embodiment which applied the joining method of the silicon wafer concerning this invention to the manufacturing process of the piezoresistance type semiconductor pressure sensor from drawing 1.
[0016]Drawing 1 shows the section of the sensor board 1 in this embodiment. In the closing-in part (diaphragm part) 2 of the sensor board 1, the piezoresistive element 3 which changes distortion into an electrical signal is embedded. Into the portion (thick part) used as a plane of

composition with the plinth board 11 shown in drawing 2. It is formed so that the diffusion prevention layer (barrier layer) 4 which prevents diffusion of Au atom may become a thickness of about 1 micrometer from thousands of A, and it is formed so that Au layer 5 may become a thickness of several micrometers by sputtering or vacuum evaporation on this diffusion prevention layer 4. By plating, the thickness of Au layer 5 may be increased further. After usually forming the diffusion prevention layer 4 and Au layer 5 in the whole sensor board 1 in a actual process, Resist grant, dry etching, resist removal, etc. are worked, These diffusion prevention layers 4 and Au layer 5 are removed selectively, chemical etching of the sensor board 1 is carried out with KOH solution, TMAH liquid (tetra methylammonium hydro oxide solution), etc. after that, and the diaphragm part 2 is formed. In addition, various publicly known processes, such as the sandblasting method and the lift-off method, can be used.

[0017]Drawing 2 shows the section of the plinth board 11 in this embodiment. The breakthrough 12 is formed in the plinth board 11 in the predetermined pitch so that it may correspond at a time to one plinth of each sensor. The breakthrough 12 is in the state joined to the sensor board 1 of drawing 1, and has the work which introduces the pressure of a fluid into the diaphragm part 2 of a sensor. The breakthrough 12 can be formed by methods, such as ultrasonic horn processing, sandblasting, and chemical etching.

[0018]Except for the portion of the breakthrough 12, the diffusion prevention layer 13 and Au layer 14 are formed in the surface of the plinth board 11. Like the sensor board 1 of drawing 1, first, the diffusion prevention layer 13 is formed so that it may become a thickness of about 1 micrometer from thousands of A, and on it, Au layer 14 is formed so that it may become a thickness of several micrometers by sputtering or vacuum evaporation. After forming the diffusion prevention layer 13 and Au layer 14 in the whole plinth board 11 in a actual process, for example, Resist grant, dry etching, resist removal, etc. will be worked, these diffusion prevention layers 13 and Au layer 14 will be removed selectively, chemical etching of the plinth board 11 will be carried out with KOH solution, TMAH liquid, etc. after that, and the breakthrough 12 will be formed. Conversely, after forming the breakthrough 12 in the plinth board 11 by chemical etching first, carry out the mask (stopgap) of this breakthrough 12 using a wax or a pillar-shaped pin, and it ranks second, Metallizing is carried out, the diffusion prevention layer 13 and Au layer 14 are formed in the portion except the portion of the breakthrough 12, and it may be made to remove what was subsequently carrying out the mask of the breakthrough 12.

[0019]Drawing 3 is a sectional view showing the state where piled up the sensor board 1 and the plinth board 11 which were produced as mentioned above, and it joined. Au layer 5 of the sensor board 1 and Au layer 14 of the plinth board 11 are piled up. Under the present circumstances, alignment is performed so that the central part of the diaphragm part 2 of the sensor board 1 and the breakthrough 12 of the plinth board 11 may be mostly in agreement. And the sensor board 1 and the plinth board 11 add the load of number kg / cm^2 to tens kg/cm^2 in the direction which pushes one another mutually in a vacuum or a nitrogen gas atmosphere of about 400-500 **. As a result, the sensor board 1 and the plinth board 11 of each other are joined by Au-Au diffusion combination.

[0020]Under the present circumstances, diffusion inside the sensor board 1 of Au layer 5 or Au atom in 14 or the plinth board 11 is controlled by the diffusion prevention layer 4 or 13. As a result, generating of the void in a plane of composition is suppressed, and firm junction is realized.

[0021]The thin film of the metal whose thermal diffusion speed is slower than Au is formed like Ti, nickel, Cr, W, aluminum, and Mo as the above-mentioned diffusion prevention layers 4 and 13. As for a metaled thermal diffusion speed, in 0.091 and nickel, according to Arrhenius' equation $D=D_0 \exp(-U/RT)$, 2.7 and Ag are [Au / 0.44 and Cu of frequency factor

D_0] 0.62 (a unit is $10^{-4}xm^2xs^{-1}$). Thermal diffusion speed is so quick that frequency factor D_0 is small. Therefore, it is preferred that frequency factor D_0 chooses sufficiently large metal like nickel compared with Au. By sputtering, a metal thin film thousands of A thick is formed.

[0022]As another embodiment, the diffusion prevention layers 4 and 13 in the above-mentioned embodiment may be formed by silicon oxide (SiO_2). By CVD (chemical vapor deposition), a SiO_2 thin film is formed so that it may become a thickness of several micrometers from thousands of A. SiO_2 is deposited on CVD at the temperature of about 800 ** or less using the gas of a $SiCl_4$-H_2-CO_2 system.

[0023]As another embodiment, the diffusion prevention layers 4 and 13 in the above-mentioned embodiment may be formed with a silicon nitride film (Si_3N_4). By plasma CVD, an Si_3N_4 thin film is formed so that it may become a thickness of thousands of A.

[0024]As another embodiment, the diffusion prevention layers 4 and 13 in the above-mentioned embodiment may be formed with a glass thin film. For example, by RF glow discharge sputtering, Pyrex glass #7740 is formed so that it may become a thickness of thousands of A. The degree of vacuum in the case of this sputtering is set as 10^{-2}torr from 10^{-1}.

[0025]The joining method of the silicon wafer by this invention can be widely applied not only to the manufacturing process of a piezoresistance type semiconductor pressure sensor but to the manufacturing process of micromachines, such as an acceleration sensor and an actuator.

[0026]

[Effect of the Invention]As explained above, according to the joining method of the silicon wafer of this invention. Since diffusion of Au atom in an Au layer is controlled by the diffusion prevention layer formed in each substrate when joining the Au layers formed in each silicon substrate, generating of the void in a plane of composition is suppressed, and firm junction is realized. If the pedestal section of a semiconductor pressure sensor is formed with the silicon wafer of the same construction material as a sensor board using this joining method, generating of the internal stress by the difference in a coefficient of thermal expansion like [when a pedestal section is formed with glass] can be prevented, and the characteristic of a sensor can be improved.

[Translation done.]

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TECHNICAL FIELD

[Field of the Invention]In the manufacturing process of micromachines, such as a piezoresistance type semiconductor pressure sensor, an acceleration sensor, and an actuator,

this invention relates to the method of joining silicon substrates in detail about the joining method of a silicon wafer.

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PRIOR ART

[Description of the Prior Art]Drawing 4 shows the structure of the piezoresistance type semiconductor pressure sensor as an example of the micromachine with which this invention is applied. This sensor has the work which takes out distortion of the sensor chip produced with minute pressure as an electrical signal. The sensor body which consists of the sensor chip 21 and the plinth glass 22 is being fixed to the plastic package 23 with the silicone or the epoxy adhesive 24 of low stress. The breakthrough 25 which introduces the pressure of a fluid into the sensor chip 21 is formed in the plastic package 23 and the plinth glass 22. The closing-in part (diaphragm part) 26 of the sensor chip 21 is equipped with the piezoresistive element (not shown) which changes into an electrical signal distortion produced with the pressure of a fluid. The plastic package 23 is PURIMORUDO the lead 27 and electrical connection of a piezoresistive element and the lead 27 is carried out with gold or the wire 28 made from aluminum.
[0003]Drawing 5 shows an example of the manufacturing process of the sensor body which consists of the above sensor chips 21 and the plinth glass 22. The sensor board (wafer) 31 in which two or more sensor chips containing the diaphragm part 33 and the piezoresistive element 34 were formed, and the glass substrate 32 made from Pyrex glass equivalent to two or more plinth glass with which the breakthrough 35 was formed are joined by anode joining. Then, it can carve into each sensor body by dicing. Thus, by manufacturing the sensor body which consists of the sensor chip 21 shown in drawing 4, and the plinth glass 22, the influence of the stress from the plastic package 23 is suppressed, and highly precise-ization of the sensor chip 21 is attained.
[0004]Anode joining of the sensor board 31 and the glass substrate 32 is performed by impressing about [400-1000V] direct current voltage between the glass substrate 32 and the sensor board 31, and impressing hundreds of g load in a vacuum or a nitrogen atmosphere of about 300-500 **. The lower heater electrode 36 is formed in the glass substrate 32 side, and it maintains to 0V potential. On the other hand, the anode pin 37 is formed in the sensor board 31 side, and about [400-1000V] direct current voltage is impressed.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention]As explained above, according to the joining method of the silicon wafer of this invention. Since diffusion of Au atom in an Au layer is controlled by the diffusion prevention layer formed in each substrate when joining the Au layers formed in each silicon substrate, generating of the void in a plane of composition is suppressed, and firm junction is realized. If the pedestal section of a semiconductor pressure sensor is formed with the silicon wafer of the same construction material as a sensor board using this joining method, generating of the internal stress by the difference in a coefficient of thermal expansion like [when a pedestal section is formed with glass] can be prevented, and the characteristic of a sensor can be improved.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]In the method of joining the sensor board 31 and the glass substrate 32 by the above anode joining, there was a problem resulting from the slight difference with the coefficient of thermal expansion of the glass substrate 32 and the coefficient of thermal expansion of the sensor board (silicon wafer) 31 used as plinth glass. That is, since the stress resulting from the difference in the above-mentioned coefficient of thermal expansion is inherent in the sensor body which consists of the sensor chip 21 which carved the sensor board 31 and the glass substrate 32 which were joined, and was made by dicing, and the plinth glass 22, a sensor body has offset voltage. Change of the temperature characteristics of an output span cannot be disregarded, either.

[0006]Then, it is possible to replace with plinth glass and to form a plinth with the silicon wafer of the same construction material as the sensor board 31. In this case, methods of joining the silicon substrate (henceforth a plinth board) used as the sensor board 31 and a plinth include the method by Au-Si eutectic bonding.
[0007]Drawing 6 shows junction to the sensor board 31 and the plinth board 41 by Au-Si eutectic bonding. First, Au layer 42 is formed in the plane of composition of the sensor board 31 by sputtering or vacuum evaporation at a thickness of several micrometers. Then, Au-Si eutectic bonding is formed by impressing the load of severalkilogram[/cm] ^{2} to tens kg/cm^2 for Au layer 42 of the sensor board 31, and the plane of composition of the plinth board 41 in piles in the atmosphere of a temperature (about 400 **) higher than the Au-Si eutectic temperature of 363 **.
[0008]Thus, if a plinth is formed with the silicon wafer of the same construction material as the sensor board 31, the problem resulting from the difference in the coefficient of thermal expansion in the case of forming a plinth with glass like before will be solved.
[0009]However, in the case of Au-Si eutectic bonding, as an arrow shows in drawing 6, Au atom in Au layer 42 is spread inside [of the sensor board 31 and the plinth board 41] silicon bulk, and, as a result, there is another problem that a void occurs in a plane of composition. When a void occurs in a plane of composition, there is a possibility that bonding strength may become weak and exfoliation by a joining interface may arise.
[0010]Like [in the case of this invention solving the above problems and forming a plinth with the silicon wafer of the same construction material as a sensor board in a pressure sensor], When joining silicon substrates, generating of the void in a plane of composition is suppressed, and it aims at providing the joining method of a silicon wafer without fear, such as exfoliation by a joining interface.

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MEANS

[Means for Solving the Problem]The 1st silicon substrate in which a circuit element was formed as for a joining method of a silicon wafer by this invention, When piling up the 2nd silicon substrate used as a plinth and joining, a diffusion prevention layer which prevents diffusion of Au to the 1st silicon substrate is formed, An Au layer is formed on it, a diffusion prevention layer which prevents diffusion of Au to the 2nd silicon substrate is formed, an Au layer is formed on it, the Au layers of the 1st and 2nd silicon substrates are piled up, predetermined load and temperature are applied, and the Au layers of both silicon substrates are joined.
[0012]According to the above joining methods, diffusion inside the 1st or 2nd silicon

substrate of Au atom in an Au layer is controlled by diffusion prevention layer formed in each silicon substrate. As a result, generating of a void in a plane of composition is suppressed, and firm junction is realized.

[0013]As for the above-mentioned diffusion prevention layer, it is preferred to form with a metal thin film containing any at least one of Ti, nickel, Cr, W, and the aluminum. Or it is also preferred to form a diffusion prevention layer with silicon oxide or a silicon nitride film. A diffusion prevention layer may be formed with a glass thin film by sputtering.

[0014]

[Embodiment of the Invention]Hereafter, the embodiment of this invention is described, referring to drawings.

[0015]Drawing 3 shows the embodiment which applied the joining method of the silicon wafer concerning this invention to the manufacturing process of the piezoresistance type semiconductor pressure sensor from drawing 1.

[0016]Drawing 1 shows the section of the sensor board 1 in this embodiment. In the closing-in part (diaphragm part) 2 of the sensor board 1, the piezoresistive element 3 which changes distortion into an electrical signal is embedded. Into the portion (thick part) used as a plane of composition with the plinth board 11 shown in drawing 2. It is formed so that the diffusion prevention layer (barrier layer) 4 which prevents diffusion of Au atom may become a thickness of about 1 micrometer from thousands of A, and it is formed so that Au layer 5 may become a thickness of several micrometers by sputtering or vacuum evaporation on this diffusion prevention layer 4. By plating, the thickness of Au layer 5 may be increased further. After usually forming the diffusion prevention layer 4 and Au layer 5 in the whole sensor board 1 in a actual process, Resist grant, dry etching, resist removal, etc. are worked, These diffusion prevention layers 4 and Au layer 5 are removed selectively, chemical etching of the sensor board 1 is carried out with KOH solution, TMAH liquid (tetra methylammonium hydro oxide solution), etc. after that, and the diaphragm part 2 is formed. In addition, various publicly known processes, such as the sandblasting method and the lift-off method, can be used.

[0017]Drawing 2 shows the section of the plinth board 11 in this embodiment. The breakthrough 12 is formed in the plinth board 11 in the predetermined pitch so that it may correspond at a time to one plinth of each sensor. The breakthrough 12 is in the state joined to the sensor board 1 of drawing 1, and has the work which introduces the pressure of a fluid into the diaphragm part 2 of a sensor. The breakthrough 12 can be formed by methods, such as ultrasonic horn processing, sandblasting, and chemical etching.

[0018]Except for the portion of the breakthrough 12, the diffusion prevention layer 13 and Au layer 14 are formed in the surface of the plinth board 11. Like the sensor board 1 of drawing 1, first, the diffusion prevention layer 13 is formed so that it may become a thickness of about 1 micrometer from thousands of A, and on it, Au layer 14 is formed so that it may become a thickness of several micrometers by sputtering or vacuum evaporation. After forming the diffusion prevention layer 13 and Au layer 14 in the whole plinth board 11 in a actual process, for example, Resist grant, dry etching, resist removal, etc. will be worked, these diffusion prevention layers 13 and Au layer 14 will be removed selectively, chemical etching of the plinth board 11 will be carried out with KOH solution, TMAH liquid, etc. after that, and the breakthrough 12 will be formed. Conversely, after forming the breakthrough 12 in the plinth board 11 by chemical etching first, carry out the mask (stopgap) of this breakthrough 12 using a wax or a pillar-shaped pin, and it ranks second, Metallizing is carried out, the diffusion prevention layer 13 and Au layer 14 are formed in the portion except the portion of the breakthrough 12, and it may be made to remove what was subsequently carrying out the mask of the breakthrough 12.

[0019]Drawing 3 is a sectional view showing the state where piled up the sensor board 1 and

the plinth board 11 which were produced as mentioned above, and it joined. Au layer 5 of the sensor board 1 and Au layer 14 of the plinth board 11 are piled up. Under the present circumstances, alignment is performed so that the central part of the diaphragm part 2 of the sensor board 1 and the breakthrough 12 of the plinth board 11 may be mostly in agreement. And the sensor board 1 and the plinth board 11 add the load of number kg / cm^2 to tens kg/cm^2 in the direction which pushes one another mutually in a vacuum or a nitrogen gas atmosphere of about 400-500 **. As a result, the sensor board 1 and the plinth board 11 of each other are joined by Au-Au diffusion combination.

[0020]Under the present circumstances, diffusion inside the sensor board 1 of Au layer 5 or Au atom in 14 or the plinth board 11 is controlled by the diffusion prevention layer 4 or 13. As a result, generating of the void in a plane of composition is suppressed, and firm junction is realized.

[0021]The thin film of the metal whose thermal diffusion speed is slower than Au is formed like Ti, nickel, Cr, W, aluminum, and Mo as the above-mentioned diffusion prevention layers 4 and 13. As for a metaled thermal diffusion speed, in 0.091 and nickel, according to Arrhenius' equation $D=D_0 \exp(-U/RT)$, 2.7 and Ag are [Au / 0.44 and Cu of frequency factor D_0] 0.62 (a unit is $10^{-4} xm^2 xs^{-1}$). Thermal diffusion speed is so quick that frequency factor D_0 is small. Therefore, it is preferred that frequency factor D_0 chooses sufficiently large metal like nickel compared with Au. By sputtering, a metal thin film thousands of A thick is formed.

[0022]As another embodiment, the diffusion prevention layers 4 and 13 in the above-mentioned embodiment may be formed by silicon oxide (SiO_2). By CVD (chemical vapor deposition), a SiO_2 thin film is formed so that it may become a thickness of several micrometers from thousands of A. SiO_2 is deposited on CVD at the temperature of about 800 ** or less using the gas of a $SiCl_4$-H_2-CO_2 system.

[0023]As another embodiment, the diffusion prevention layers 4 and 13 in the above-mentioned embodiment may be formed with a silicon nitride film (Si_3N_4). By plasma CVD, an Si_3N_4 thin film is formed so that it may become a thickness of thousands of A.

[0024]As another embodiment, the diffusion prevention layers 4 and 13 in the above-mentioned embodiment may be formed with a glass thin film. For example, by RF glow discharge sputtering, Pyrex glass #7740 is formed so that it may become a thickness of thousands of A. The degree of vacuum in the case of this sputtering is set as 10^{-2}torr from 10^{-1}.

[0025]The joining method of the silicon wafer by this invention can be widely applied not only to the manufacturing process of a piezoresistance type semiconductor pressure sensor but to the manufacturing process of micromachines, such as an acceleration sensor and an actuator.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a sectional view of the sensor board in the piezoresistance type semiconductor pressure sensor manufactured using the joining method of this invention.
[Drawing 2]It is a sectional view of the plinth board in a piezoresistance type semiconductor pressure sensor.
[Drawing 3]It is a sectional view showing the state where piled up the sensor board and the plinth board and it joined.
[Drawing 4]It is a sectional view of the conventional piezoresistance type semiconductor pressure sensor.
[Drawing 5]It is a sectional view showing an example of the manufacturing process of the sensor body which consists of a conventional sensor chip and plinth glass.
[Drawing 6]It is a sectional view showing another example (comparative example) of the manufacturing process of a sensor body.
[Description of Notations]
1 Sensor board (the 1st silicon substrate)
2 Closing-in part (diaphragm part)
3 Piezoresistive element
4 and 13 Diffusion prevention layer
5, 14 Au layers
11 Plinth board (the 2nd silicon substrate)
12 Breakthrough

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DESCRIPTION OF DRAWINGS

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[Drawing 2]It is a sectional view of the plinth board in a piezoresistance type semiconductor pressure sensor.
[Drawing 3]It is a sectional view showing the state where piled up the sensor board and the

plinth board and it joined.
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[Drawing 5]It is a sectional view showing an example of the manufacturing process of the sensor body which consists of a conventional sensor chip and plinth glass.
[Drawing 6]It is a sectional view showing another example (comparative example) of the manufacturing process of a sensor body.
[Description of Notations]
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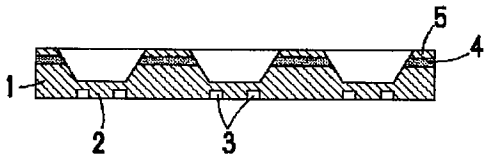
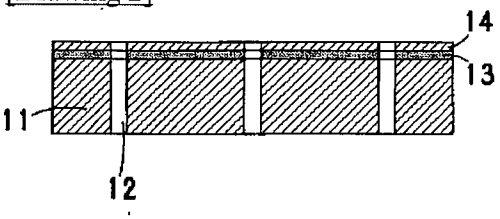
DRAWINGS

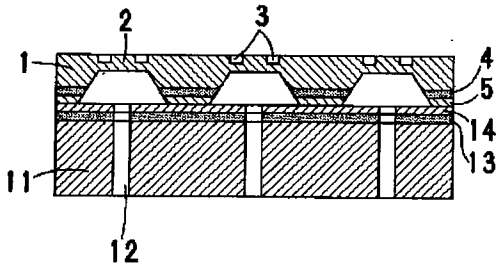
[Drawing 1]



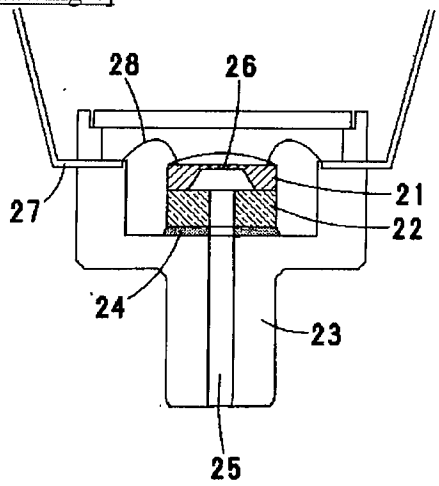
[Drawing 2]



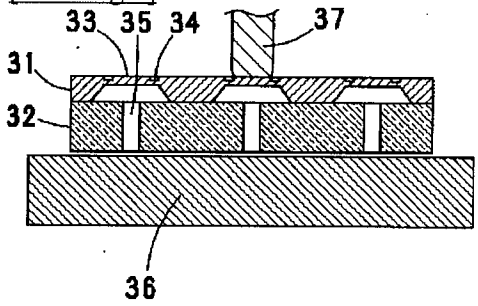
[Drawing 3]



[Drawing 4]



[Drawing 5]



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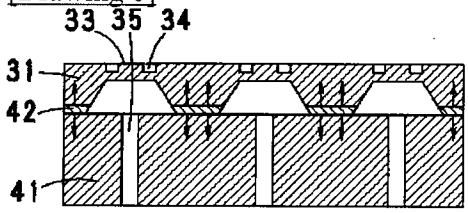

[Translation done.]

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(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
特開2001－150398
（P2001－150398A）
(43)公開日　平成13年６月５日(2001.6.5)

(51)Int.Cl.⁷	識別記号	ＦＩ		テーマコード（参考）
Ｂ８１Ｃ　3/00		Ｂ８１Ｃ　3/00		２Ｆ０５５
Ｇ０１Ｌ　9/04	１０１	Ｇ０１Ｌ　9/04	１０１	
Ｇ０１Ｐ　15/12		Ｇ０１Ｐ　15/12		
Ｈ０１Ｌ　21/02		Ｈ０１Ｌ　21/02	Ｂ	
41/08		41/08	Ｚ	

審査請求　未請求　請求項の数５　ＯＬ　（全５頁）

(21)出願番号　特願平11－335481
(22)出願日　平成11年11月26日(1999.11.26)

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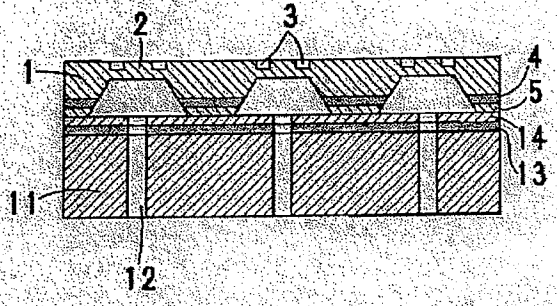
最終頁に続く

(54)【発明の名称】　シリコンウェハの接合方法

(57)【要約】
【課題】　シリコン基板同士を接合する際に、接合面におけるボイドの発生を抑え、接合界面での剥離等のおそれがないシリコンウェハの接合方法を提供する。
【解決手段】　回路素子３が形成された第１のシリコン基板１と、台座となる第２のシリコン基板１１とを重ね合わせて接合する際に、第１のシリコン基板１にＡｕの拡散を防止する拡散防止層４を形成し、その上にＡｕ層５を形成し、第２のシリコン基板にＡｕの拡散を防止する拡散防止層１３を形成し、その上にＡｕ層１４を形成し、第１及び第２のシリコン基板１，１１のＡｕ層５，１４同士を重ね、所定の荷重及び温度を加えて両シリコン基板１，１１のＡｕ層５，１４同士を接合する。拡散防止層は、Ｔｉ，Ｎｉ，Ｃｒ，Ｗ，Ａｌ等の金属薄膜、シリコン酸化膜、シリコン窒化膜、又はガラス薄膜で形成する。



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【特許請求の範囲】

【請求項１】回路素子が形成された第１のシリコン基板と、台座となる第２のシリコン基板とを重ね合わせて接合するシリコンウェハの接合方法であって、

前記第１のシリコン基板にＡｕの拡散を防止する拡散防止層を形成し、その上にＡｕ層を形成し、

前記第２のシリコン基板にＡｕの拡散を防止する拡散防止層を形成し、その上にＡｕ層を形成し、

前記第１及び第２のシリコン基板のＡｕ層同士を重ね、所定の荷重及び温度を加えて両シリコン基板のＡｕ層同士を接合することを特徴とするシリコンウェハの接合方法。

【請求項２】前記拡散防止層をＴｉ，Ｎｉ，Ｃｒ，Ｗ，Ａｌの少なくともいずれか１つを含む金属薄膜で形成することを特徴とする請求項１記載のシリコンウェハの接合方法。

【請求項３】前記拡散防止層をシリコン酸化膜で形成することを特徴とする請求項１記載のシリコンウェハの接合方法。

【請求項４】前記拡散防止層をシリコン窒化膜で形成することを特徴とする請求項１記載のシリコンウェハの接合方法。

【請求項５】前記拡散防止層をスパッタリングによるガラス薄膜で形成することを特徴とする請求項１記載のシリコンウェハの接合方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明はシリコンウェハの接合方法に関し、詳しくは、ピエゾ抵抗型半導体圧力センサ、加速度センサ、アクチュエータ等のマイクロマシンの製造プロセスにおいて、シリコン基板同士を接合する方法に関する。

【０００２】

【従来の技術】図４は、本発明が適用されるマイクロマシンの一例として、ピエゾ抵抗型半導体圧力センサの構造を示している。このセンサは微小圧力によって生ずるセンサチップの歪みを電気信号として取り出す働きを有する。センサチップ２１と台座ガラス２２からなるセンサ本体がプラスチックパッケージ２３に低応力のシリコーン又はエポキシ系接着剤２４で固定されている。プラスチックパッケージ２３及び台座ガラス２２には、センサチップ２１に流体の圧力を導入する貫通孔２５が設けられている。センサチップ２１の肉薄部（ダイヤフラム部）２６には流体の圧力によって生ずる歪みを電気信号に変換するピエゾ抵抗素子（図示せず）が備えられている。プラスチックパッケージ２３にはリード２７がプリモールドされており、金又はアルミ製のワイヤ２８によってピエゾ抵抗素子とリード２７とが電気接続されている。

【０００３】図５は、上記のようなセンサチップ２１と台座ガラス２２からなるセンサ本体の製造プロセスの一例を示している。ダイヤフラム部３３及びピエゾ抵抗素子３４を含む複数のセンサチップが形成されたセンサ基板（ウェハ）３１と貫通孔３５が形成された複数の台座ガラスに相当するパイレックスガラス製のガラス基板３２とが陽極接合によって接合される。その後、ダイシングによって個々のセンサ本体に切り分けられる。このようにして、図４に示したセンサチップ２１と台座ガラス２２からなるセンサ本体を製造することにより、プラスチックパッケージ２３からの応力の影響を抑え、センサチップ２１の高精度化が可能になる。

【０００４】センサ基板３１とガラス基板３２との陽極接合は、約３００～５００℃の真空又は窒素雰囲気中で、ガラス基板３２とセンサ基板３１との間に４００～１０００Ｖ程度の直流電圧を印加し、数百グラムの荷重を印加することによって行われる。ガラス基板３２側に下ヒータ電極３６を設け、０Ｖ電位に維持する。一方、センサ基板３１側に陽極ピン３７を設け、４００～１０００Ｖ程度の直流電圧を印加する。

【０００５】

【発明が解決しようとする課題】上記のような陽極接合によってセンサ基板３１とガラス基板３２とを接合する方法では、台座ガラスとなるガラス基板３２の熱膨張係数とセンサ基板（シリコンウェハ）３１の熱膨張係数とのわずかな相違に起因する問題があった。すなわち，接合されたセンサ基板３１とガラス基板３２とをダイシングによって切り分けてできたセンサチップ２１と台座ガラス２２からなるセンサ本体には、上記の熱膨張係数の違いに起因する応力が内在しているために、センサ本体がオフセット電圧を有する。また、出力スパンの温度特性の変動も無視できない。

【０００６】そこで、台座ガラスに代えて、センサ基板３１と同じ材質のシリコンウェハで台座を形成することが考えられる。この場合、センサ基板３１と台座となるシリコン基板（以下、台座基板という）を接合する方法として、Ａｕ－Ｓｉ共晶結合による方法がある。

【０００７】図６は、Ａｕ－Ｓｉ共晶結合によるセンサ基板３１と台座基板４１との接合を示している。まず、センサ基板３１の接合面にスパッタリング又は蒸着によってＡｕ層４２を数μｍの厚さに形成する。この後、Ａｕ－Ｓｉ共晶温度３６３℃より高い温度（約４００℃）の雰囲気中でセンサ基板３１のＡｕ層４２と台座基板４１の接合面とを重ねて数ｋｇ／ｃｍ²から数十ｋｇ／ｃｍ²の加重を印加することにより、Ａｕ－Ｓｉ共晶結合を形成する。

【０００８】このように、センサ基板３１と同じ材質のシリコンウェハで台座を形成すれば、従来のようにガラスで台座を形成する場合の熱膨張係数の違いに起因する問題は解消される。

【０００９】しかしながら、Ａｕ－Ｓｉ共晶結合の場

合、図６中に矢印で示すように、Ａｕ層４２中のＡｕ原子がセンサ基板３１及び台座基板４１のシリコンバルク内部へ拡散し、その結果、接合面にボイドが発生するといった別の問題がある。接合面にボイドが発生すると、接合強度が弱くなり接合界面での剥離が生ずるおそれがある。

【００１０】本発明は上記のような問題を解決し、圧力センサにおいてセンサ基板と同じ材質のシリコンウェハで台座を形成する場合のように、シリコン基板同士を接合する際に、接合面におけるボイドの発生を抑え、接合界面での剥離等のおそれがないシリコンウェハの接合方法を提供することを目的とする。

【００１１】

【課題を解決するための手段】本発明によるシリコンウェハの接合方法は、回路素子が形成された第１のシリコン基板と、台座となる第２のシリコン基板とを重ね合わせて接合する際に、第１のシリコン基板にＡｕの拡散を防止する拡散防止層を形成し、その上にＡｕ層を形成し、第２のシリコン基板にＡｕの拡散を防止する拡散防止層を形成し、その上にＡｕ層を形成し、第１及び第２のシリコン基板のＡｕ層同士を重ね、所定の荷重及び温度を加えて両シリコン基板のＡｕ層同士を接合することを特徴とする。

【００１２】上記のような接合方法によれば、Ａｕ層中のＡｕ原子の第１又は第２のシリコン基板の内部への拡散がそれぞれのシリコン基板に形成された拡散防止層によって抑制される。その結果、接合面におけるボイドの発生が抑えられ、強固な接合が実現する。

【００１３】上記の拡散防止層は、Ｔｉ，Ｎｉ，Ｃｒ，Ｗ，Ａｌの少なくともいずれか１つを含む金属薄膜で形成することが好ましい。あるいは、拡散防止層をシリコン酸化膜又はシリコン窒化膜で形成することも好ましい。拡散防止層をスパッタリングによるガラス薄膜で形成してもよい。

【００１４】

【発明の実施の形態】以下、図面を参照しながら本発明の実施形態を説明する。

【００１５】図１から図３は、本発明に係るシリコンウェハの接合方法をピエゾ抵抗型半導体圧力センサの製造プロセスに適用した実施形態を示している。

【００１６】図１は本実施形態におけるセンサ基板１の断面を示している。センサ基板１の肉薄部（ダイヤフラム部）２には歪みを電気信号に変換するピエゾ抵抗素子３が埋め込まれている。図２に示す台座基板１１との接合面となる部分（肉厚部）には、Ａｕ原子の拡散を防止する拡散防止層（バリア層）４が数千オングストロームから約１μｍの厚さになるように形成され、この拡散防止層４の上にＡｕ層５がスパッタリング又は蒸着により数μｍの厚さになるように形成されている。メッキによって、Ａｕ層５の厚さをさらに増加してもよい。実際のプロセスでは通常、センサ基板１の全体に拡散防止層４及びＡｕ層５を形成した後、レジスト付与、ドライエッチング、レジスト除去等の作業を行って、これら拡散防止層４及びＡｕ層５を部分的に除去し、その後ＫＯＨ水溶液、ＴＭＡＨ液（tetra methylammonium hydro oxide solution）等でセンサ基板１をケミカルエッチングして、ダイヤフラム部２を形成する。その他、サンドブラスト法、リフトオフ法等の種々の公知のプロセスを使用することができる。

【００１７】図２は、本実施形態における台座基板１１の断面を示している。台座基板１１には、各センサの台座に１個ずつ対応するように、貫通孔１２が所定のピッチで形成されている。貫通孔１２は、図１のセンサ基板１と接合した状態で、流体の圧力をセンサのダイヤフラム部２に導入する働きを有する。貫通孔１２は、超音波ホーン加工、サンドブラスト、ケミカルエッチング等の方法によって形成することができる。

【００１８】台座基板１１の表面には、貫通孔１２の部分を除いて、拡散防止層１３及びＡｕ層１４が形成されている。図１のセンサ基板１と同様に、まず拡散防止層１３を数千オングストロームから約１μｍの厚さになるように形成し、その上にＡｕ層１４をスパッタリング又は蒸着により数μｍの厚さになるように形成する。実際のプロセスでは、例えば、台座基板１１の全体に拡散防止層１３及びＡｕ層１４を形成した後、レジスト付与、ドライエッチング、レジスト除去等の作業を行って、これら拡散防止層１３及びＡｕ層１４を部分的に除去し、その後ＫＯＨ水溶液、ＴＭＡＨ液等で台座基板１１をケミカルエッチングして、貫通孔１２を形成することになる。また、逆に、まず台座基板１１にケミカルエッチングで貫通孔１２を形成した後、この貫通孔１２をワックスや柱状ピンを用いてマスク（穴埋め）し、次いで、メタライズして拡散防止層１３及びＡｕ層１４を、貫通孔１２の部分を除いた部分に形成し、次いで貫通孔１２をマスクしていたものを取り除くようにしてもよい。

【００１９】図３は、上記のようにして作製したセンサ基板１と台座基板１１とを重ね合わせて接合した状態を示す断面図である。センサ基板１のＡｕ層５と台座基板１１のＡｕ層１４とを重ねる。この際、センサ基板１のダイヤフラム部２の中心部と台座基板１１の貫通孔１２とがほぼ一致するように位置合わせが行われる。そして、約４００～５００℃の真空又は窒素ガス雰囲気中で、センサ基板１と台座基板１１とが互いに押し合う方向に数ｋｇ／ｃｍ²から数十ｋｇ／ｃｍ²の荷重を加える。この結果、Ａｕ－Ａｕ拡散結合によってセンサ基板１と台座基板１１とが互いに接合される。

【００２０】この際、Ａｕ層５又は１４中のＡｕ原子のセンサ基板１又は台座基板１１の内部への拡散が拡散防止層４又は１３によって抑制される。その結果、接合面におけるボイドの発生が抑えられ、強固な接合が実現す

る。

【００２１】上記の拡散防止層４，１３として、Ｔｉ，Ｎｉ，Ｃｒ，Ｗ，Ａｌ，Ｍｏのように、Ａｕより熱拡散速度が遅い金属の薄膜を形成する。金属の熱拡散速度は、アレニウスの式$D=D_0\exp(-U/RT)$に従い、頻度因子D_0は、Ａｕが０．０９１、Ｎｉが２．７、Ａｇが０．４４、Ｃｕが０．６２（単位は$10^{-4}\times m^2\times s^{-1}$）である。頻度因子$D_0$が小さいほど、熱拡散速度が速い。したがって、Ｎｉのように、Ａｕに比べて頻度因数D_0が十分大きい金属を選択することが好ましい。スパッタリングにより、数千オングストロームの厚さの金属薄膜を形成する。

【００２２】別の実施形態として、上記の実施形態における拡散防止層４，１３をシリコン酸化膜（SiO_2）で形成してもよい。ＣＶＤ（化学蒸着法）により、SiO_2薄膜を数千オングストロームから数μｍの厚さになるように形成する。ＣＶＤには$SiCl_4-H_2-CO_2$系のガスを用い、約８００℃以下の温度でSiO_2を堆積する。

【００２３】更に別の実施形態として、上記の実施形態における拡散防止層４，１３をシリコン窒化膜（Si_3N_4）で形成してもよい。プラズマＣＶＤにより、Si_3N_4薄膜を数千オングストロームの厚さになるように形成する。

【００２４】更に別の実施形態として、上記の実施形態における拡散防止層４，１３をガラス薄膜で形成してもよい。例えばパイレックスガラス＃７７４０をＲＦグロー放電スパッタリングにより、数千オングストロームの厚さになるように形成する。このスパッタリングの際の真空度は10^{-3}から10^{-2}torrに設定する。

【００２５】なお、本発明によるシリコンウェハの接合方法はピエゾ抵抗型半導体圧力センサの製造プロセスに限らず、加速度センサやアクチュエータ等のマイクロマシンの製造プロセスにも広く適用することが可能である。

＊【００２６】

【発明の効果】以上に説明したように、本発明のシリコンウェハの接合方法によれば、それぞれのシリコン基板に形成したＡｕ層同士を接合する際に、Ａｕ層中のＡｕ原子の拡散がそれぞれの基板に形成された拡散防止層によって抑制されるので、接合面におけるボイドの発生が抑えられ、強固な接合が実現する。また、この接合方法を用いて半導体圧力センサの台座部分をセンサ基板と同じ材質のシリコンウェハで形成すれば、ガラスで台座部分を形成したときのような熱膨張係数の違いによる内部応力の発生を防ぎ、センサの特性を向上することができる。

【図面の簡単な説明】

【図１】本発明の接合方法を用いて製造するピエゾ抵抗型半導体圧力センサにおけるセンサ基板の断面図である。

【図２】ピエゾ抵抗型半導体圧力センサにおける台座基板の断面図である。

【図３】センサ基板と台座基板とを重ね合わせて接合した状態を示す断面図である。

【図４】従来のピエゾ抵抗型半導体圧力センサの断面図である。

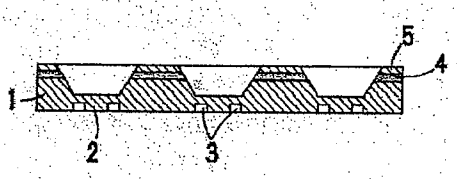
【図５】従来のセンサチップと台座ガラスからなるセンサ本体の製造プロセスの一例を示す断面図である。

【図６】センサ本体の製造プロセスの別の例（比較例）を示す断面図である。

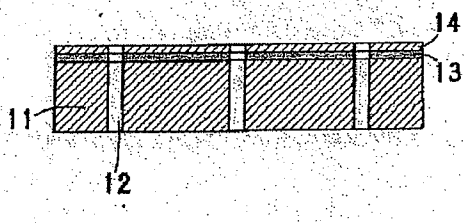
【符号の説明】

１　センサ基板(第１のシリコン基板)
２　肉薄部（ダイヤフラム部）
３　ピエゾ抵抗素子
４，１３　拡散防止層
５，１４　Ａｕ層
１１　台座基板(第２のシリコン基板)
１２　貫通孔

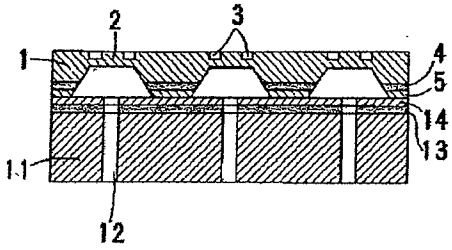
【図１】



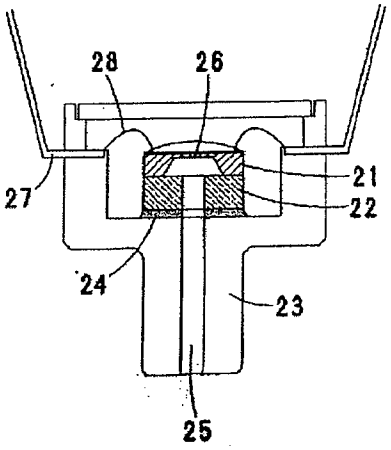
【図２】



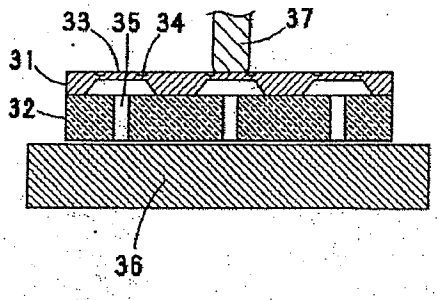
【図３】



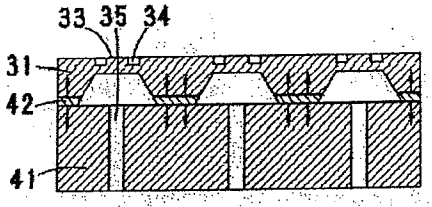
【図４】



【図５】



【図６】



フロントページの続き

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Ｆターム(参考)　2F055 AA40 BB20 CC02 DD05 EE13 FF11 FF49 GG01 GG13